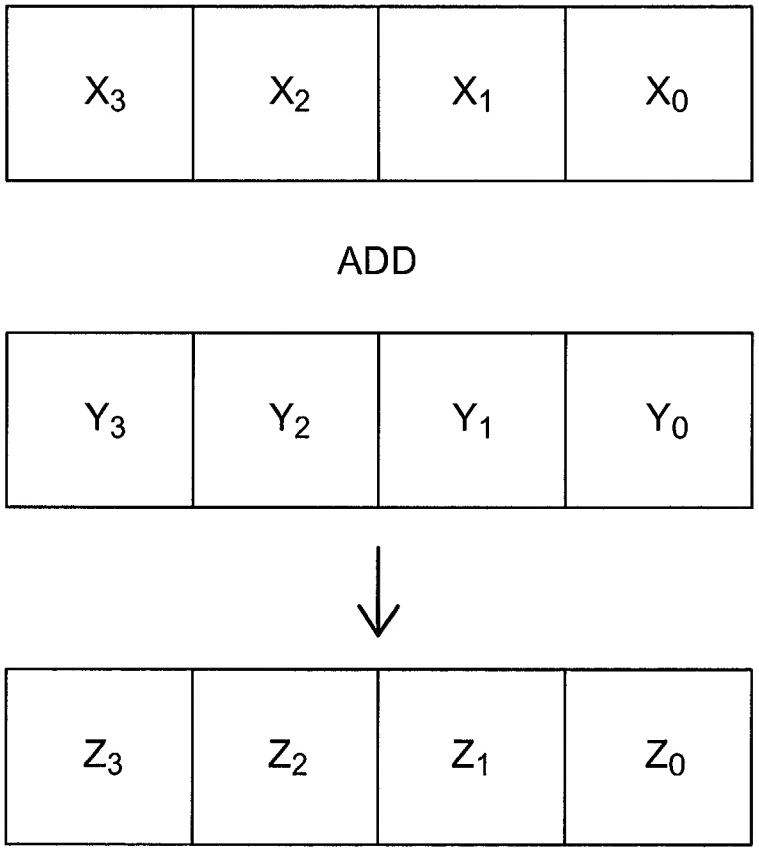

FIG. 1
PRIOR ART

TOSOSO" ZT32586O

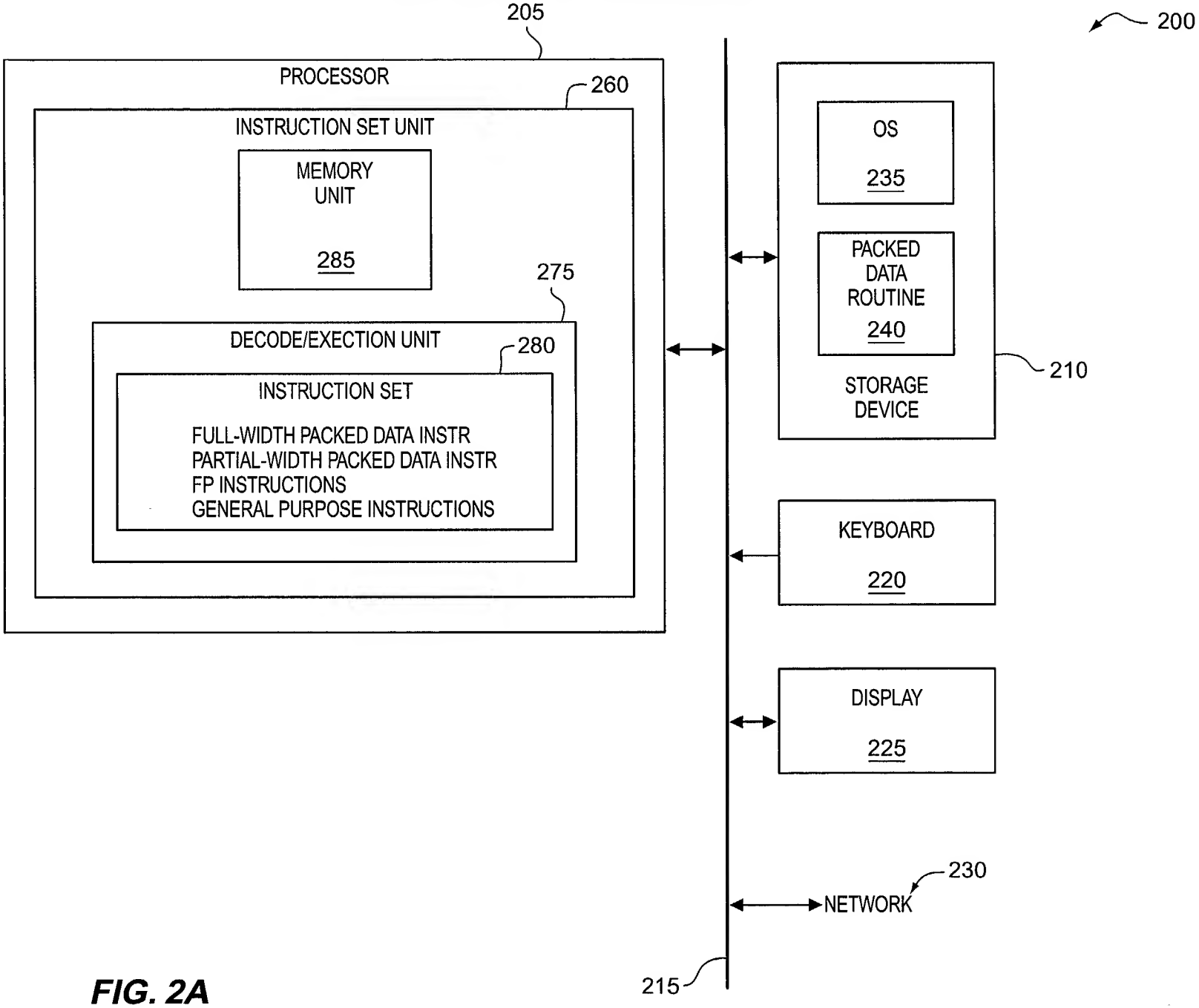

FIG. 2A

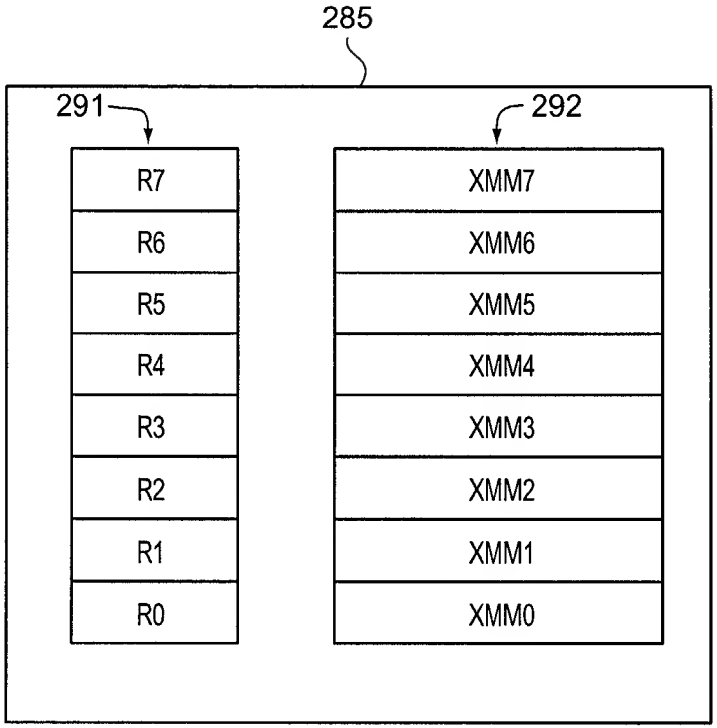
285
291
292
R7
R6
R5
R4
R3
R2
R1
R0
XMM7
XMM6
XMM5
XMM4
XMM3
XMM2
XMM1
XMM0

FIG. 2B

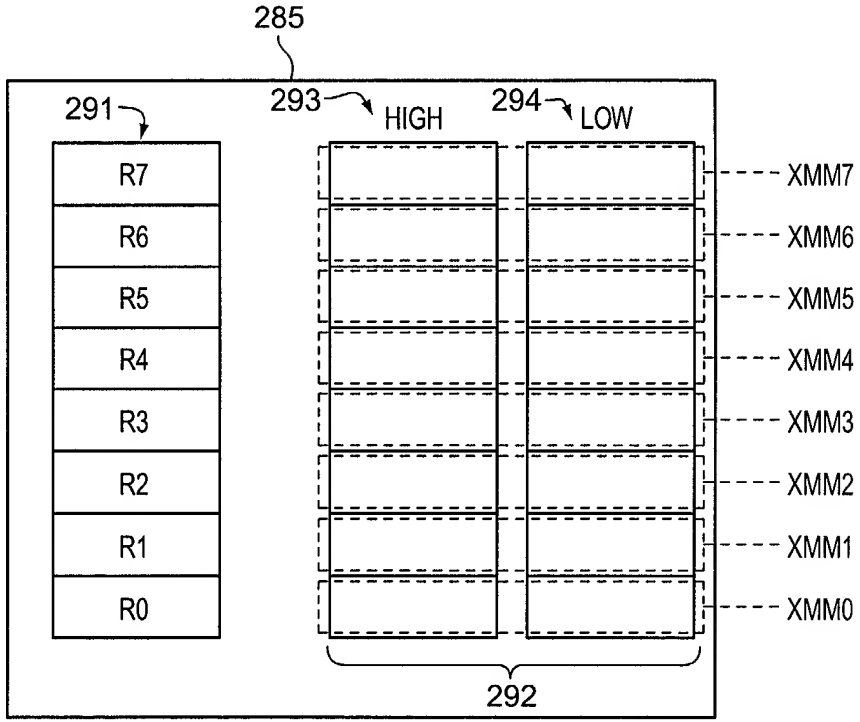
285
291
293
HIGH
294
LOW
R7
R6
R5
R4
R3
R2
R1
R0
XMM7
XMM6
XMM5
XMM4
XMM3
XMM2
XMM1
XMM0
292

FIG. 2C

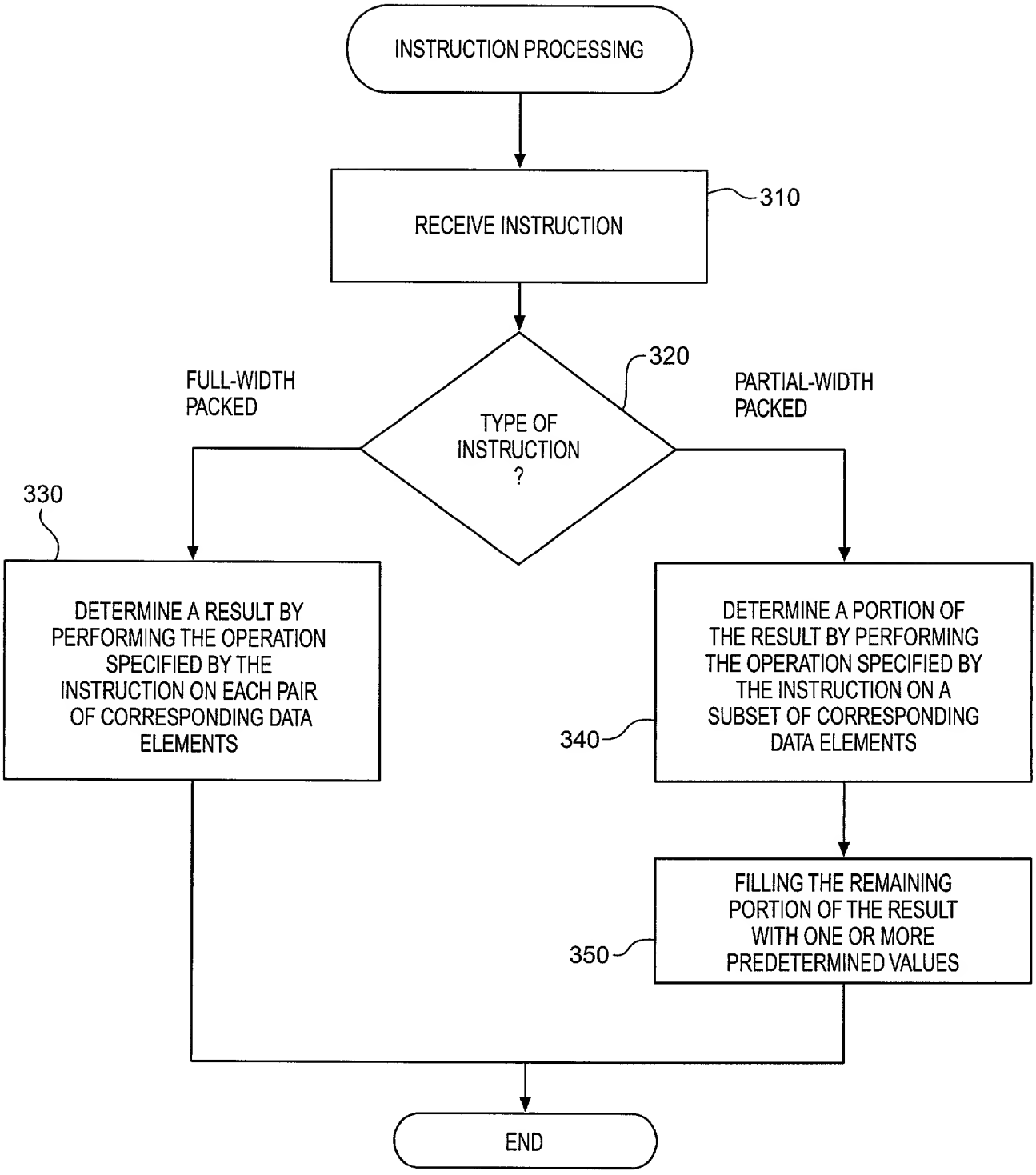
INSTRUCTION PROCESSING
RECEIVE INSTRUCTION
310
320
TYPE OF INSTRUCTION ?
FULL-WIDTH PACKED
PARTIAL-WIDTH PACKED
330
DETERMINE A RESULT BY PERFORMING THE OPERATION SPECIFIED BY THE INSTRUCTION ON EACH PAIR OF CORRESPONDING DATA ELEMENTS
340
DETERMINE A PORTION OF THE RESULT BY PERFORMING THE OPERATION SPECIFIED BY THE INSTRUCTION ON A SUBSET OF CORRESPONDING DATA ELEMENTS
350
FILLING THE REMAINING PORTION OF THE RESULT WITH ONE OR MORE PREDETERMINED VALUES
END

FIG. 3

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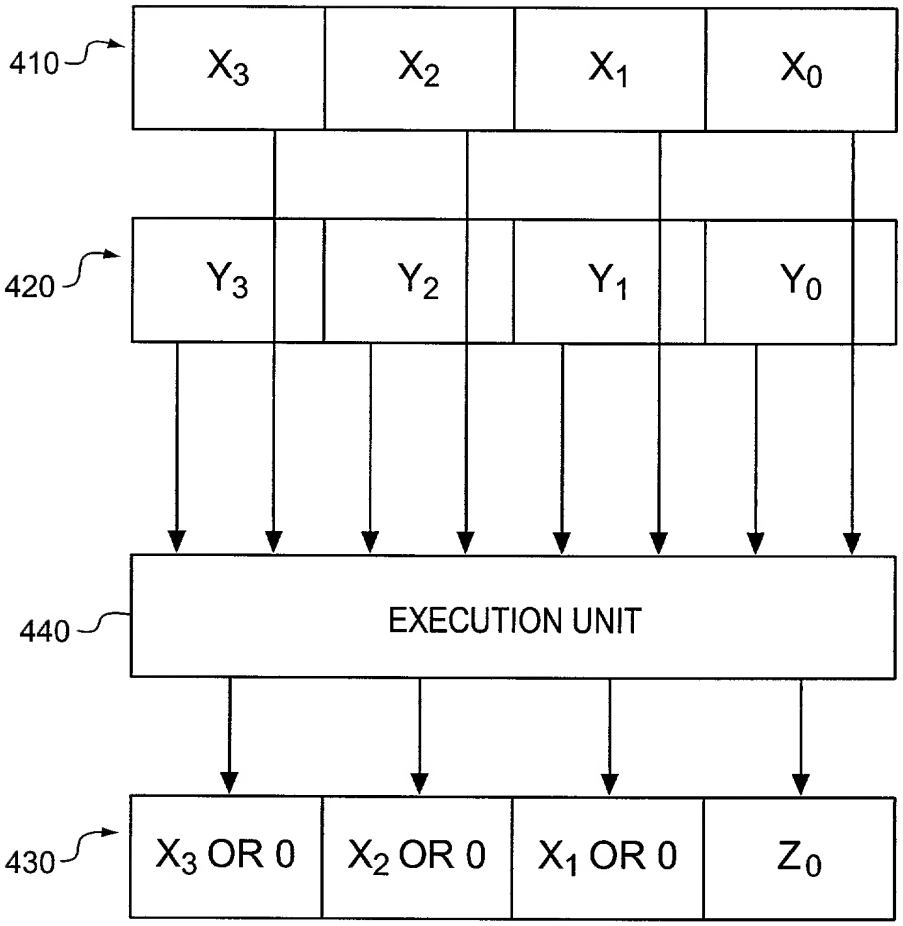

FIG. 4

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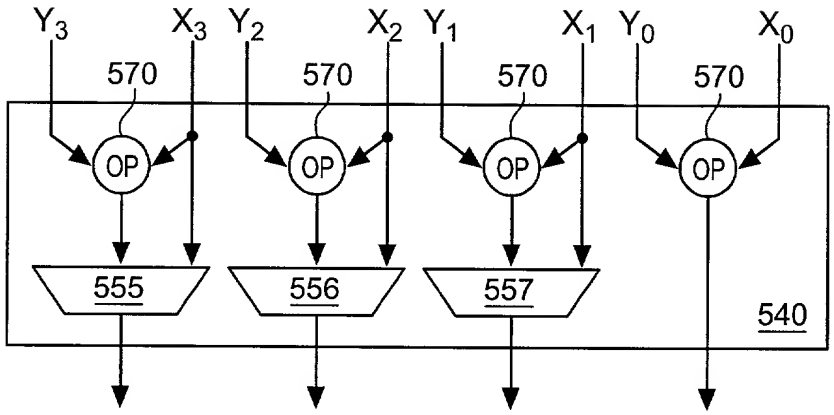


FIG. 5A

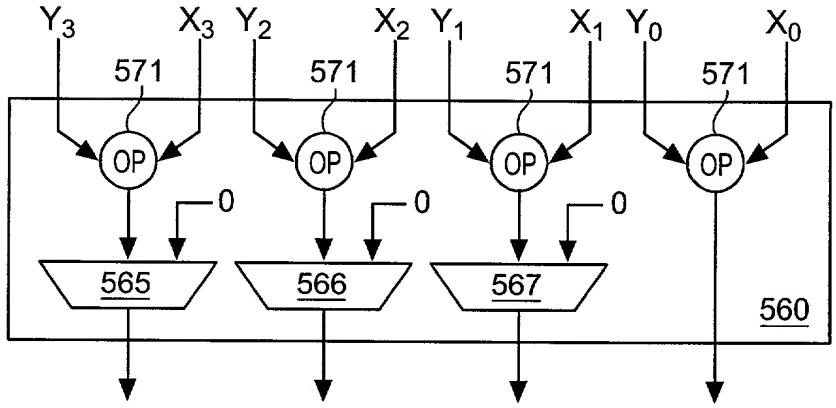


FIG. 5B

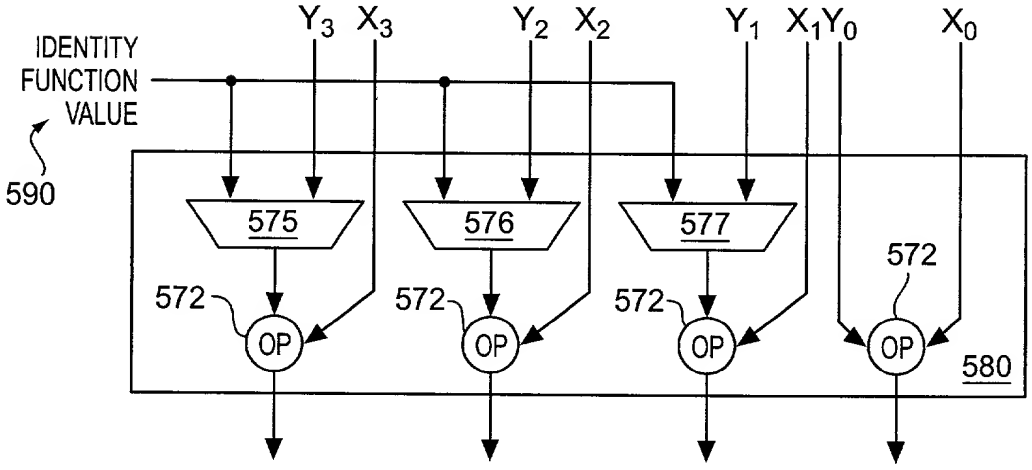


FIG. 5C

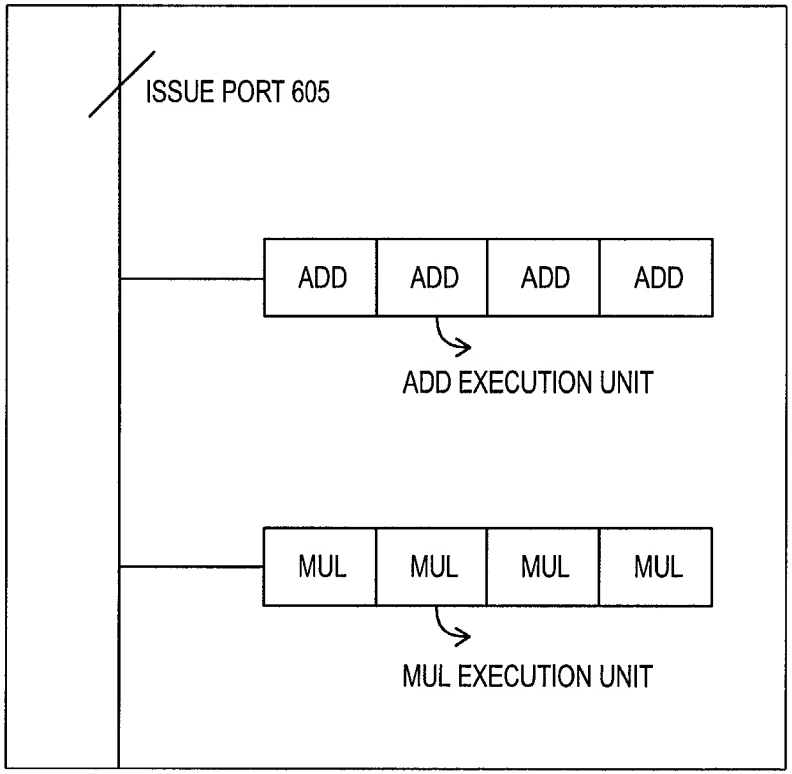

ISSUE PORT 605
ADD
ADD
ADD
ADD
ADD EXECUTION UNIT
MUL
MUL
MUL
MUL
MUL EXECUTION UNIT

FIG. 6

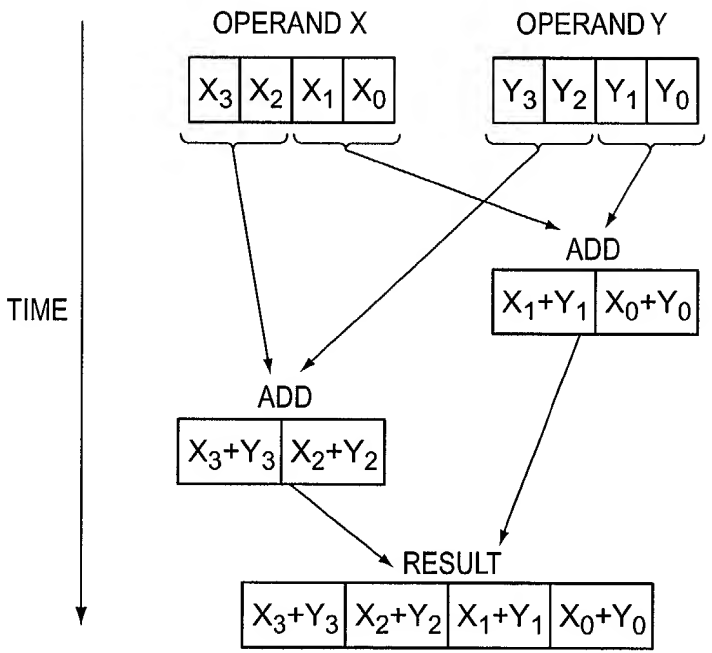
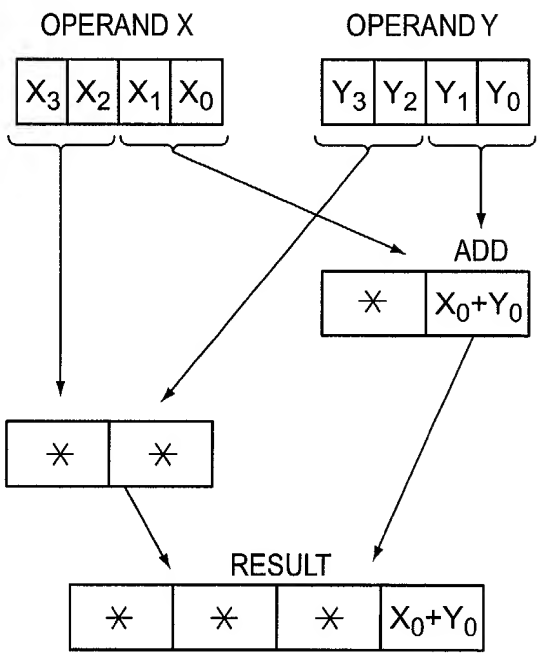


FIG. 7A



✳ = CORRESPONDING DATA ELEMENT IN X OR Y, NaN, 0, OR OTHER PREDETERMINED VALUE

FIG. 7B

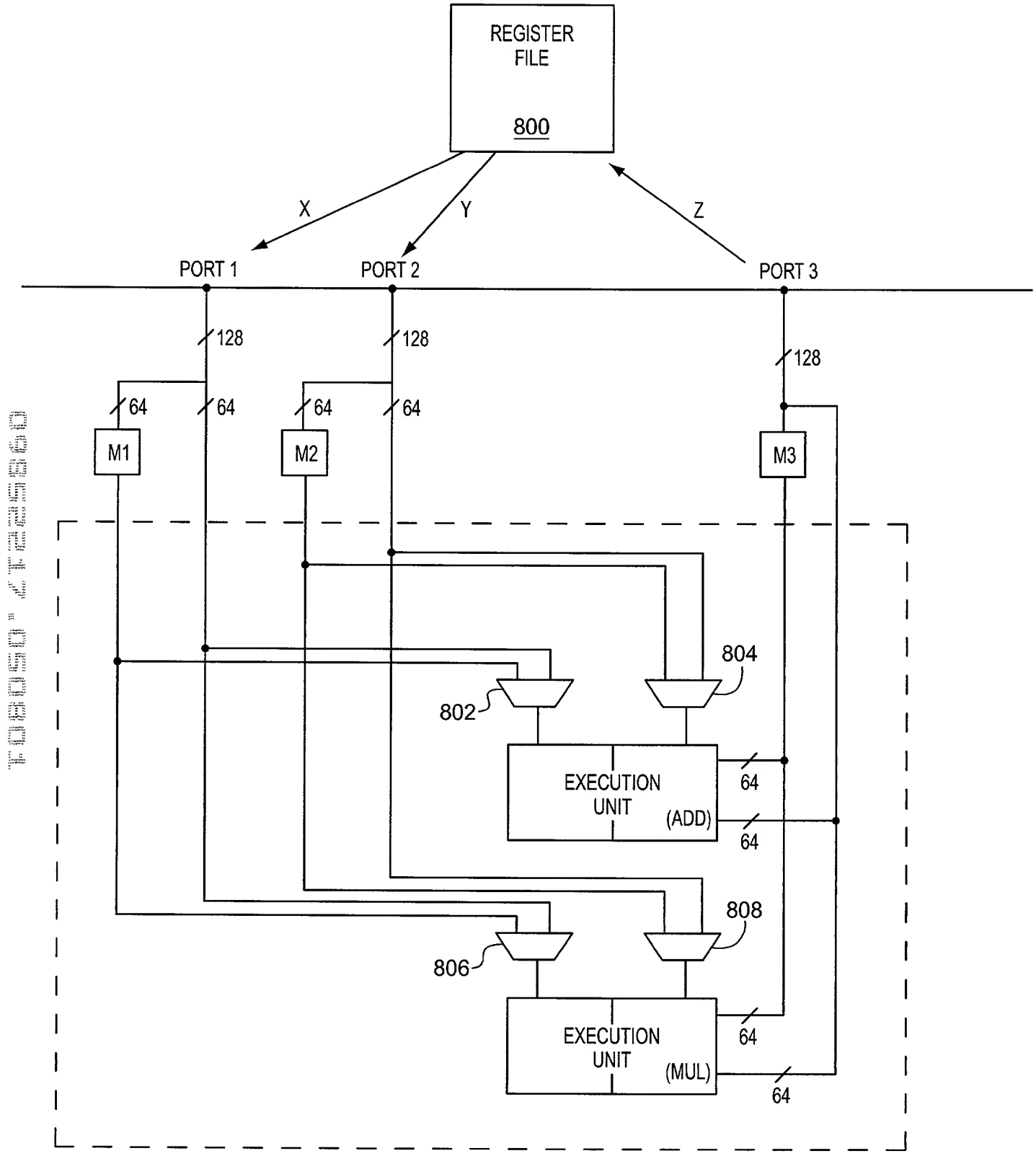

REGISTER FILE
800
X
Y
Z
PORT 1
PORT 2
PORT 3
128
128
128
64
64
64
64
M1
M2
M3
804
802
EXECUTION UNIT
(ADD)
64
64
808
806
EXECUTION UNIT
(MUL)
64
64

FIG. 8A

TIME	128-BIT INSTRUCTION	PERFORMED ON 64-BIT DATA
T	ADD X, Y	ADD X_0 Y_0 ADD X_1 Y_1
T+1		ADD X_2 Y_2 ADD X_3 Y_3
T+1	MUL X, Y	MUL X_0 Y_0 MUL X_1 Y_1
T+2		MUL X_2 Y_2 MUL X_3 Y_3

FIG. 8B

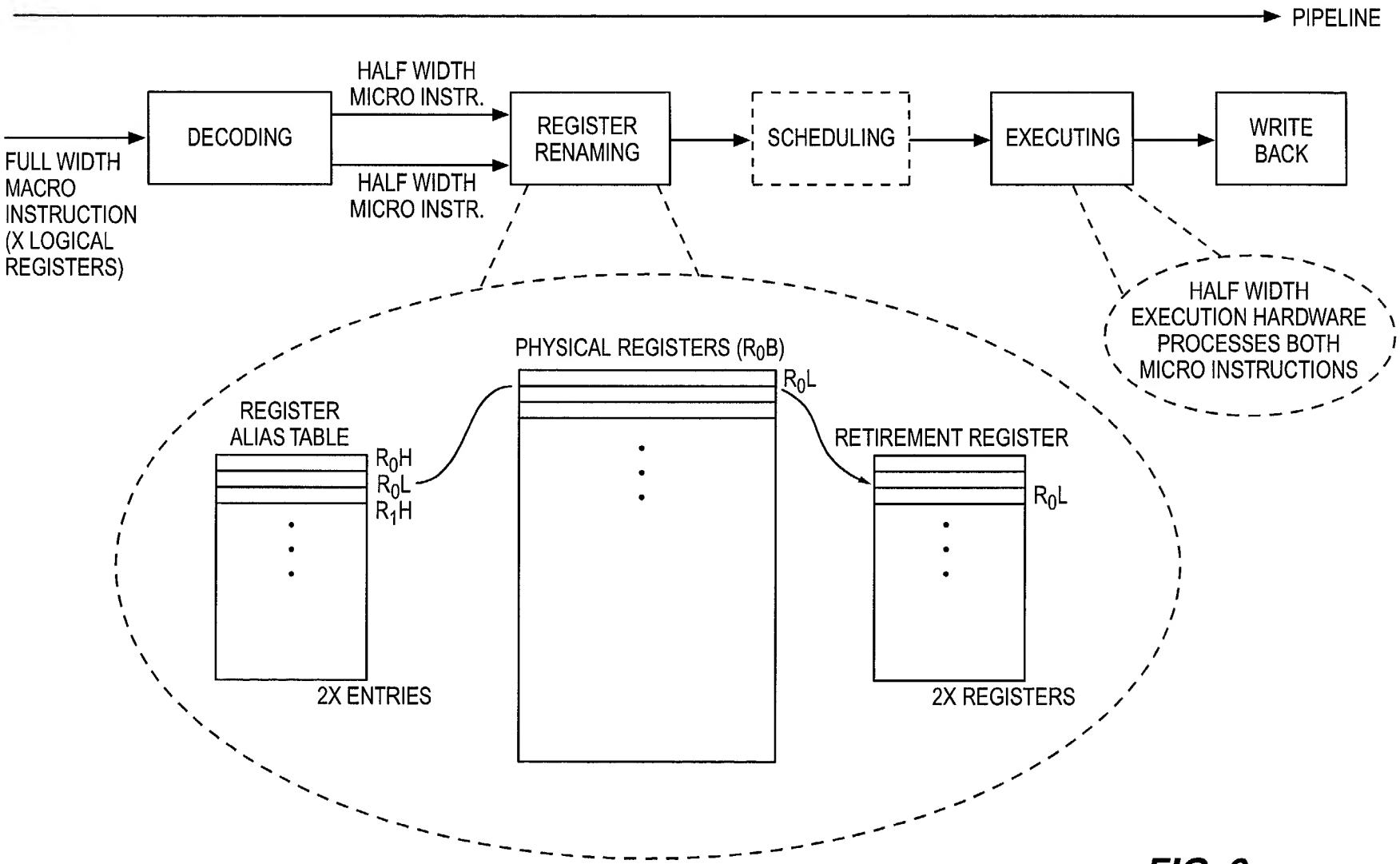

PIPELINE
FULL WIDTH MACRO INSTRUCTION (X LOGICAL REGISTERS)
DECODING
HALF WIDTH MICRO INSTR.
HALF WIDTH MICRO INSTR.
REGISTER RENAMING
SCHEDULING
EXECUTING
WRITE BACK
HALF WIDTH EXECUTION HARDWARE PROCESSES BOTH MICRO INSTRUCTIONS
PHYSICAL REGISTERS (R_0B)
R_0L
REGISTER ALIAS TABLE
R_0H
R_0L
R_1H
2X ENTRIES
RETIREMENT REGISTER
R_0L
2X REGISTERS

FIG. 9

TIME	128-BIT INSTRUCTION	64-BIT INSTRUCTION
T	ADD X, Y	ADD X_L , Y_L
T + N		ADD X_H , Y_H

FIG. 10

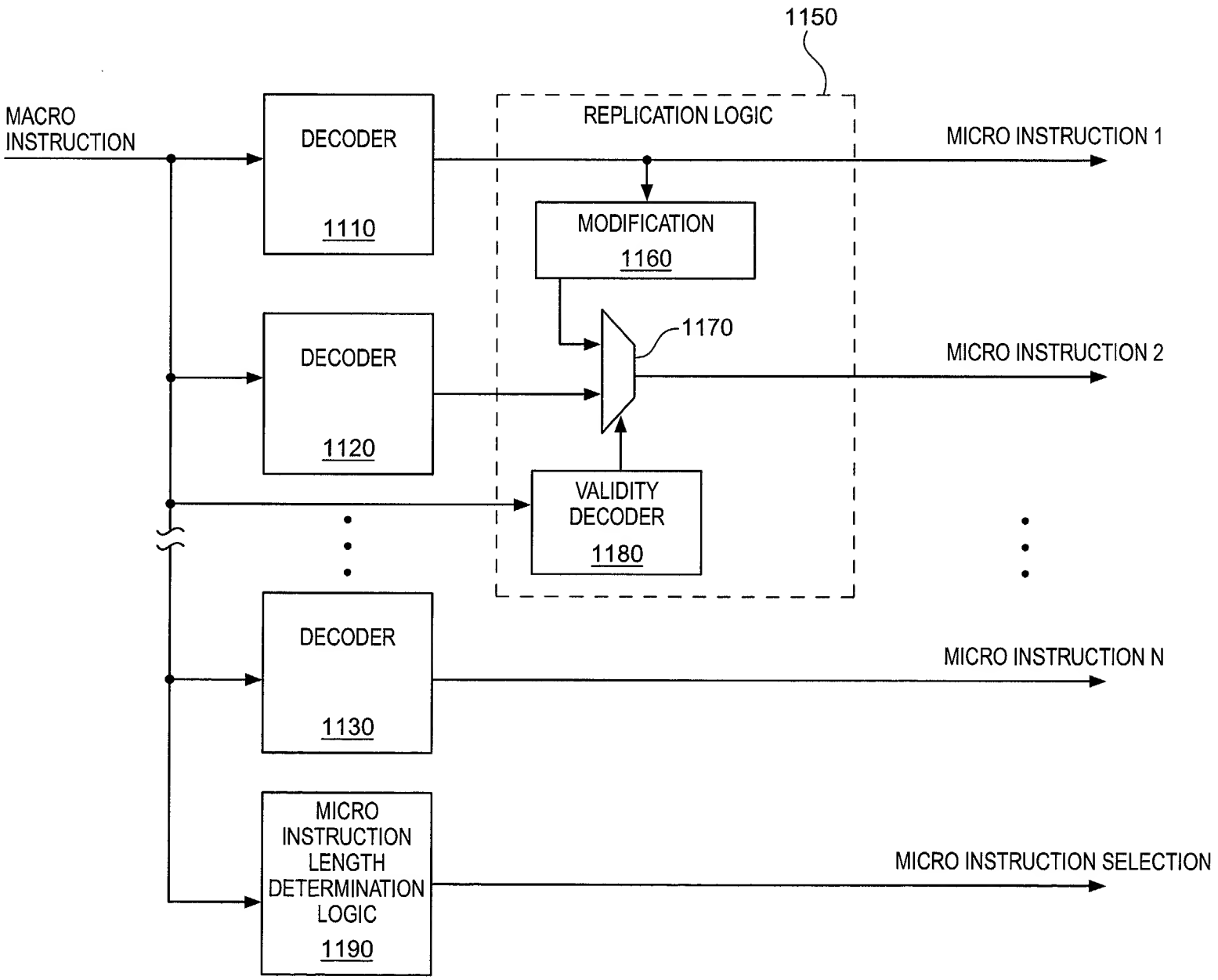

1150
MACRO INSTRUCTION
DECODER
1110
REPLICATION LOGIC
MICRO INSTRUCTION 1
MODIFICATION
1160
DECODER
1120
1170
MICRO INSTRUCTION 2
VALIDITY DECODER
1180
DECODER
1130
MICRO INSTRUCTION N
MICRO INSTRUCTION LENGTH DETERMINATION LOGIC
1190
MICRO INSTRUCTION SELECTION

FIG. 11